

Kojigaya et al. [45] Date of Patent: * Jun. 9, 1990

[54] SEMICONDUCTOR MEMORY

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[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[1*] Notice: The portion of the term of this patent subsequent to Oct. 25, 2009 has been disclaimed.

[31] Appl. No.: 288,314

[22] Filed: Oct. 11, 1988

Related U.S. Application Data

[62] Division of Ser. No. 873,072, Jun. 24, 1986, Pat. No. 4,792,452.

[50] Foreign Application Priority Data

Jun. 14, 1985 [JP] Japan 60-137738

[91] Int. Cl. * G11C 7/00

[52] U.S. Cl. 365/204; 365/205

[58] Field of Search 365/149; 365; 203; 204; 365/210

[56] References Cited

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[4,601,017 7/1984 Mochizuki et al. 365/203 X
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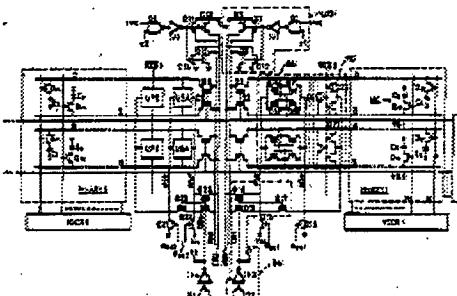
K. Kawamoto et al., "A 256 Kb CMOS Pseudo SRAM", 1984 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 276-277.

Primary Examiner—Joseph A. Popak
Attorney, Agent or Firm—Antonelli, Terry & Wandy

[37] ABSTRACT

A dynamic RAM is arranged such that a common data line in each of the non-selected ones of the divided memory arrays is connected to a pair of common source lines of a sense amplifier corresponding to the memory array concerned, whereby the potential of the common data line is set at a medium level which is substantially equal to the potential of the data lines by utilizing the medium potential of the pair of common source lines and a relatively large parasitic capacity thereof, thereby maintaining the data lines at the half-precharge level. The pair of common source lines are allotted to each other during the non-select period of the memory arrays, so that the common source lines have a medium level which is substantially equal to the half-precharge level of the data lines.

20 Claims, 3 Drawing Sheets



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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20020048204	20020425	49	Semiconductor integrated circuit device	365/200		
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20010030889	20011018	91	Nonvolatile semiconductor memory device	365/185.05	365/185.18; 365/185.29	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6438036 B2	20020820	92	Nonvolatile semiconductor memory device	365/185.22	365/185.18	
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6407954 B2	20020618	17	Nonvolatile semiconductor memory device	365/201	365/189.05; 365/230.08	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6404694 B2	20020611	43	Semiconductor memory device with address comparing	365/230.03	365/189.01	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6259629 B1	20010710	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6181600 B1	20010130	94	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6157576 A	20001205	94	Nonvolatile semiconductor memory device	365/185.29	365/185.21; 365/185.22	
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6134169 A	20001017	15	Semiconductor memory device	365/222	365/189.04	
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6064606 A	20000516	48	Semiconductor integrated circuit device	365/200	365/63	
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6016273 A	20000118	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18	

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
12	<input type="checkbox"/>	<input type="checkbox"/>	US 5991200 A	19991123	93	Nonvolatile semiconductor memory device	365/185.18	365/185.19; 365/185.22;	
13	<input type="checkbox"/>	<input type="checkbox"/>	US 5959894 A	19990928	90	Nonvolatile semiconductor memory device	365/185.29	365/185.18; 365/185.22	
14	<input type="checkbox"/>	<input type="checkbox"/>	US 5949715 A	19990907	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.24	
15	<input type="checkbox"/>	<input type="checkbox"/>	US 5943278 A	19990824	10	SRAM with fast write capability	365/204	365/189.05; 365/189.11;	
16	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5917752 A	19990629	92	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24	
17	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5844842 A	19981201	93	Nonvolatile semiconductor memory device	365/185.24	365/185.29	
18	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5818785 A	19981006	17	Semiconductor memory device having a plurality of banks	365/230.03	365/189.05; 365/230.06	
19	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5781476 A	19980714	93	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.19;	
20	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5777921 A	19980707	26	Non-volatile semiconductor memory device	365/145	365/222	
21	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5767544 A	19980616	47	Semiconductor integrated circuit device	257/318	365/200	
22	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5615151 A	19970325	21	Semiconductor integrated circuit operable and	365/185.18	365/185.03; 365/185.06;	

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DB: USPAT:US:PGPUB:EP1:JPO:DERWENT:IBM:TOB Print Highlight items in list

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U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
23	<input checked="" type="checkbox"/>	US 5570241 A	19961029	15	single channel, multiple head servo writing with	360/46	360/51; 360/68	
24	<input checked="" type="checkbox"/>	US 5467314 A	19951114	8	Method of testing an address multiplexed dynamic RAM	365/201	365/193; 365/230.02	
25	<input checked="" type="checkbox"/>	US 5457335 A	19951010	46	Floating gate FET with hydrogen barrier shield	257/318	257/630; 257/640;	
26	<input checked="" type="checkbox"/>	US 5444663 A	19950822	22	Semiconductor integrated circuit operable and	365/226	365/189.09	
27	<input checked="" type="checkbox"/>	US 5422858 A	19950606		Semiconductor integrated circuit	365/233	365/220; 365/239	
28	<input checked="" type="checkbox"/>	US 5398047 A	19950314		Semiconductor integrated circuit device including	345/519	345/530; 365/230.05	
29	<input checked="" type="checkbox"/>	US 5331596 A	19940719		Address multiplexed dynamic RAM having a test mode	365/201	365/193; 365/230.02;	
30	<input checked="" type="checkbox"/>	US 5117393 A	19920526		Method of testing memory cells in an address	365/201	365/193; 365/233;	
31	<input checked="" type="checkbox"/>	US 5097446 A	19920317		Nonvolatile semiconductor memory device	365/185.12	365/185.11; 365/185.21;	
32	<input type="checkbox"/>	US 5065363 A	19911112	24	Semiconductor storage device	365/154	365/189.05	
33	<input checked="" type="checkbox"/>	US 5020028 A	19910528	13	Four transistor static RAM cell	365/154	257/369; 257/903	

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the bit line capacitance charging operation. A write buffer operation, i.e., causing the capacitance component on a bit line to temporarily hold write charge information (high-speed bit line capacitance charging operation), can be performed at a relatively fast speed and is similar to a normal data write operation with respect to a DRAM (Dynamic Access memory). For the information write operation to a memory cell transistor within a short period of time, a write operation is viewed as being written to the memory (EEPROM) (a portion of the second object).

Detailed Description Text - DETX (19):

FIG. 1 shows part of the arrangement of the EEPROM. An actual memory cell array includes many main/sub bit lines, word lines, selection gate lines, selection transistors, memory cell transistors, and the like. These memory cell transistors are arranged in the form of a matrix. Row and column decoder circuits (peripheral circuits) for specifying a predetermined memory cell in accordance with an external address input are connected to this memory cell matrix. A bit line precharge circuit and a sense amplifier for reading stored data from a specified memory cell transistor are connected to each of a

United States Patent 5,623,444
Goto et al. Aug. 22, 1997

CN: ELECTRICALLY ERASABLE ROM WITH FIELD-DRIVEN MEMORY CELL TRANSISTOR

UNITED STATES PATENT DOCUMENTS

1991-1994: 5,525,034, 5,525,035, 5,525,036, 5,525,037, 5,525,038, 5,525,039, 5,525,040, 5,525,041, 5,525,042, 5,525,043, 5,525,044, 5,525,045, 5,525,046, 5,525,047, 5,525,048, 5,525,049, 5,525,050, 5,525,051, 5,525,052, 5,525,053, 5,525,054, 5,525,055, 5,525,056, 5,525,057, 5,525,058, 5,525,059, 5,525,060, 5,525,061, 5,525,062, 5,525,063, 5,525,064, 5,525,065, 5,525,066, 5,525,067, 5,525,068, 5,525,069, 5,525,070, 5,525,071, 5,525,072, 5,525,073, 5,525,074, 5,525,075, 5,525,076, 5,525,077, 5,525,078, 5,525,079, 5,525,080, 5,525,081, 5,525,082, 5,525,083, 5,525,084, 5,525,085, 5,525,086, 5,525,087, 5,525,088, 5,525,089, 5,525,090, 5,525,091, 5,525,092, 5,525,093, 5,525,094, 5,525,095, 5,525,096, 5,525,097, 5,525,098, 5,525,099, 5,525,100, 5,525,101, 5,525,102, 5,525,103, 5,525,104, 5,525,105, 5,525,106, 5,525,107, 5,525,108, 5,525,109, 5,525,110, 5,525,111, 5,525,112, 5,525,113, 5,525,114, 5,525,115, 5,525,116, 5,525,117, 5,525,118, 5,525,119, 5,525,120, 5,525,121, 5,525,122, 5,525,123, 5,525,124, 5,525,125, 5,525,126, 5,525,127, 5,525,128, 5,525,129, 5,525,130, 5,525,131, 5,525,132, 5,525,133, 5,525,134, 5,525,135, 5,525,136, 5,525,137, 5,525,138, 5,525,139, 5,525,140, 5,525,141, 5,525,142, 5,525,143, 5,525,144, 5,525,145, 5,525,146, 5,525,147, 5,525,148, 5,525,149, 5,525,150, 5,525,151, 5,525,152, 5,525,153, 5,525,154, 5,525,155, 5,525,156, 5,525,157, 5,525,158, 5,525,159, 5,525,160, 5,525,161, 5,525,162, 5,525,163, 5,525,164, 5,525,165, 5,525,166, 5,525,167, 5,525,168, 5,525,169, 5,525,170, 5,525,171, 5,525,172, 5,525,173, 5,525,174, 5,525,175, 5,525,176, 5,525,177, 5,525,178, 5,525,179, 5,525,180, 5,525,181, 5,525,182, 5,525,183, 5,525,184, 5,525,185, 5,525,186, 5,525,187, 5,525,188, 5,525,189, 5,525,190, 5,525,191, 5,525,192, 5,525,193, 5,525,194, 5,525,195, 5,525,196, 5,525,197, 5,525,198, 5,525,199, 5,525,200, 5,525,201, 5,525,202, 5,525,203, 5,525,204, 5,525,205, 5,525,206, 5,525,207, 5,525,208, 5,525,209, 5,525,210, 5,525,211, 5,525,212, 5,525,213, 5,525,214, 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5,525,761, 5,525,762, 5,525,763, 5,525,764, 5,525,765, 5,525,766, 5,525,767, 5,525,768, 5,525,769, 5,525,770, 5,525,771, 5,525,772, 5,525,773, 5,525,774, 5,525,775, 5,525,776, 5,525,777, 5,525,778, 5,525,779, 5,525,780, 5,525,781, 5,525,782, 5,525,783, 5,525,784, 5,525,785, 5,525,786, 5,525,787, 5,525,788, 5,525,789, 5,525,790, 5,525,791, 5,525,792, 5,525,793, 5,525,794, 5,525,795, 5,525,796, 5,525,797, 5,525,798, 5,525,799, 5,525,800, 5,525,801, 5,525,802, 5,525,803, 5,525,804, 5,525,805, 5,525,806, 5,525,807, 5,525,808, 5,525,809, 5,525,810, 5,525,811, 5,525,812, 5,525,813, 5,525,814, 5,525,815, 5,525,816, 5,525,817, 5,525,818, 5,525,819, 5,525,820, 5,525,821, 5,525,822, 5,525,823, 5,525,824, 5,525,825, 5,525,826, 5,525,827, 5,525,828, 5,525,829, 5,525,830, 5,525,831, 5,525,832, 5,525,833, 5,525,834, 5,525,835, 5,525,836, 5,525,837, 5,525,838, 5,525,839, 5,525,840, 5,525,841, 5,525,842, 5,525,843, 5,525,844, 5,525,845, 5,525,846, 5,525,847, 5,525,848, 5,525,849, 5,525,850, 5,525,851, 5,525,852, 5,525,853, 5,525,854, 5,525,855, 5,525,856, 5,525,857, 5,525,858, 5,525,859, 5,525,860, 5,525,861, 5,525,862, 5,525,863, 5,525,864, 5,525,865, 5,525,866, 5,525,867, 5,525,868, 5,525,869, 5,525,870, 5,525,871, 5,525,872, 5,525,873, 5,525,874, 5,525,875, 5,525,876, 5,525,877, 5,525,878, 5,525,879, 5,525,880, 5,525,881, 5,525,882, 5,525,883, 5,525,884, 5,525,885, 5,525,886, 5,525,887, 5,525,888, 5,525,889, 5,525,890, 5,525,891, 5,525,892, 5,525,893, 5,525,894, 5,525,895, 5,525,896, 5,525,897, 5,525,898, 5,525,899, 5,525,900, 5,525,901, 5,525,902, 5,525,903, 5,525,904, 5,525,905, 5,525,906, 5,525,907, 5,525,908, 5,525,909, 5,525,910, 5,525,911, 5,525,912, 5,525,913, 5,525,914, 5,525,915, 5,525,916, 5,525,917, 5,525,918, 5,525,919, 5,525,920, 5,525,921, 5,525,922, 5,525,923, 5,525,924, 5,525,925, 5,525,926, 5,525,927, 5,525,928, 5,525,929, 5,525,930, 5,525,931, 5,525,932, 5,525,933, 5,525,934, 5,525,935, 5,525,936, 5,525,937, 5,525,938, 5,525,939, 5,525,940, 5,525,941, 5,525,942, 5,525,943, 5,525,944, 5,525,945, 5,525,946, 5,525,947, 5,525,948, 5,525,949, 5,525,950, 5,525,951, 5,525,952, 5,525,953, 5,525,954, 5,525,955, 5,525,956, 5,525,957, 5,525,958, 5,525,959, 5,525,960, 5,525,961, 5,525,962, 5,525,963, 5,525,964, 5,525,965, 5,525,966, 5,525,967, 5,525,968, 5,525,969, 5,525,970, 5,525,971, 5,525,972, 5,525,973, 5,525,974, 5,525,975, 5,525,976, 5,525,977, 5,525,978, 5,525,979, 5,525,980, 5,525,981, 5,525,982, 5,525,983, 5,525,984, 5,525,985, 5,525,986, 5,525,987, 5,525,988, 5,525,989, 5,525,990, 5,525,991, 5,525,992, 5,525,993, 5,525,994, 5,525,995, 5,525,996, 5,525,997, 5,525,998, 5,525,999, 5,525,1000, 5,525,1001, 5,525,1002, 5,525,1003, 5,525,1004, 5,525,1005, 5,525,1006, 5,525,1007, 5,525,1008, 5,525,1009, 5,525,1010, 5,525,1011, 5,525,1012, 5,5



Further comprises a shared p-sense amplifier, a shared n-sense amplifier, and a plurality of n-channel depletion transistors selectively coupling the plurality of pairs of digit lines to the shared p-sense amplifier and the n-sense amplifier.

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RELATED ART
FIG. 4

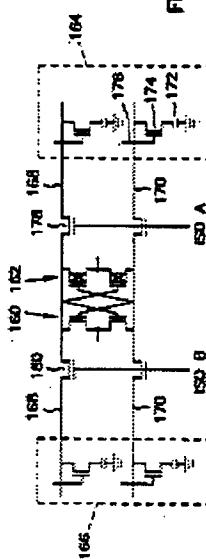
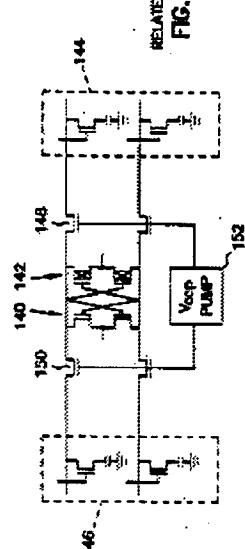


FIG. 5

Detailed Description Text - DETX (3):

In the most general sense, a memory circuit comprises memory cells which store data. Depending upon the type of memory, this data can be read, or read and written. That is, some memories are read-only while others allow data to be read, manipulated, and re-written. Because many types of memories store data as a charge on a capacitor, sense amplifiers are implemented to detect small charges and amplify the charge for further processing. FIG. 1 is a simplified block diagram of a memory array 100 having memory cells 101 connected to a sense amplifier 102. The sense amplifier 102 can be used to sense a charge stored on the memory cells and write the charge back to the memory.

Detail Test Image HTML KWIC

Detail Test Image HTML Full

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Kajigaya et al. [45] Date of Patent: Oct. 25, 1988

[54] SEMICONDUCTOR MEMORY

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[21] Appl. No.: 878,072

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[30] Foreign Application Priority Data

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[11] Int. Cl. 4 G11C 7/00

[52] U.S. Cl. 365/209, 365/205, 365/203, 365/210

[58] Field of Search 365/149, 203, 205, 203, 365/210

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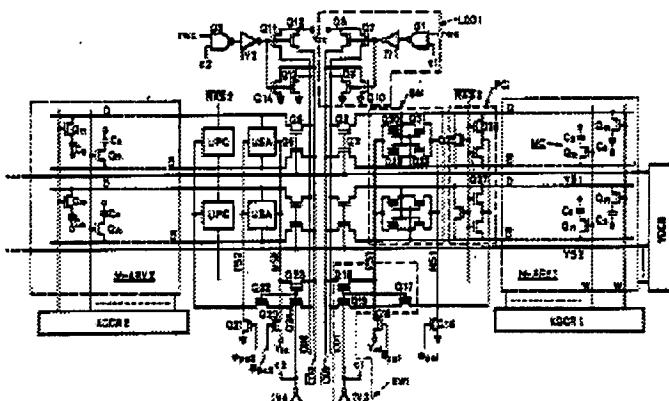
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Attorney, Agent or Firms—Antonelli, Terry & Wards

[37] ABSTRACT

A dynamic RAM is arranged such that a common data line in each of the non-selected ones of the divided memory arrays is connected to a pair of common source lines of a sense amplifier corresponding to the memory array concerned, whereby the potential of the common data line is set at a medium level which is substantially equal to the potential of the data lines by utilizing the medium potential of the pair of common source lines and a relatively large parasitic capacity thereof, thereby maintaining the data lines at the half-precharge level. The pair of common source lines are shorted to each other during the non-select period of the memory arrays so that the common source lines have a medium level which is substantially equal to the half-precharge level of the data lines.

18 Claims, 3 Drawing Sheets



Details Text Image HTML Full

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